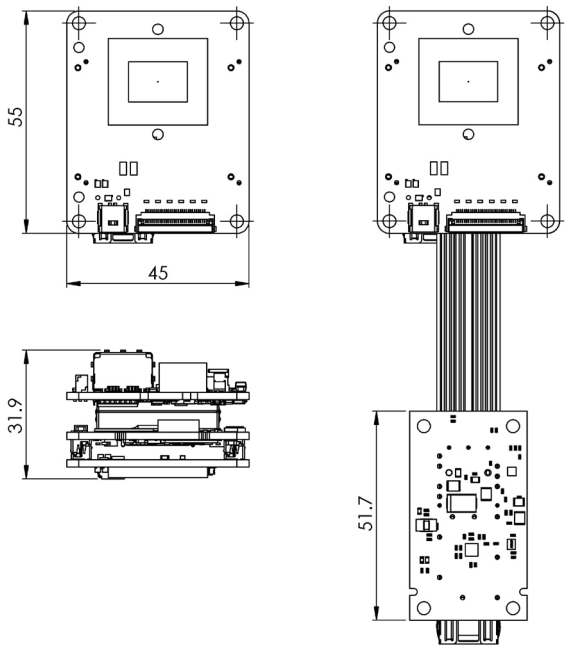
SPINOSAURUS EVO



SPINOSAURUS EVO is a highly customizable and user-programmable FPGA based on high-speed smart cameras, is a high-end FPGA camera with a Xilinx Zynq FPGA and high-speed imaging sensor and a 10 Gigabit Ethernet. It includes high-performance ARM System-on-Chip (SoC) technology combined with a turbocharged industrial SONY imaging sensor.

With high-performance FPGA System-on-Chip (SoC) technology, the Spinosaurus EVO camera family opens new dimensions in computer vision. It is a global shutter industrial camera with high frame rates and an open FPGA architecture. With FPGA processing power the image processing algorithms can run in real-time on the camera. Just add your imagination.

Spinosaurus EVO includes full customizable and user-programmable open reference design for a high-speed, FPGA-based camera and application development system. Its emphasis is on an open hardware/software development model, high-frame rates, real-time image processing on FPGA and modern graphical user interface support on the PC side.

A suite of versatile and high-performance tools for Xilinx Zynq Ultrascale+ SoC FPGA are available to develop algorithms and process data in real-time. Images are acquired by SONY PREGIUS GEN3 sensors with a SLVS-EC v1.2 interface (8x 2.3 Gbps) achieving a brilliant image at very high speed.

The on-board 4GB LPDDR4 memory with 9.6 GB/s of bandwidth enables usage of complex buffered image processing.

The reference design can be easily edited with standard Xilinx Vivado tools. OptoMotive´s custom IP cores seamlessly integrate inside the Xilinx Vivado toolchain. A large portion of FPGA (PL) is free for the programming and development of new algorithms or the implementation of additional IP cores. The 1.2 GHz Dual Core ARM Cortex A53 Programmable Subsystem runs a Linux OS with custom-made EVO control and streaming stack (including Zero-copy TCP/IP stack). The SoC also includes dual 600MHz Cortex R5 processors which are free for user data processing. User applications or custom data post-processing can be easily added to any existing design.

APPLICATIONS:

- Laser triangulation - with a ready-made Peak detector on-board image processing core;
- Motion capture - with a ready-made BLOB detector or Running Length Encoder (RLE) on-board image processing core;
- Industrial process automation - to count, detect, check, verify, read, inspect and test different products, levels, components, etc. at incredible speed;
- Industrial quality control - to inspect defects, cracks or surface blemishes, size, position, dimension and color, foreign objects or quality and
- General R&D.

KEY CAMERA FEATURES

SPINOSAURUS EVO					
Resolution	0.5 MP	2.0 MP	2.8 MP	1.7 MP	7.1 MP
Active Pixels (HxV)	816 x 624	1632 x 1248	1944 x 1427	1608 x 1104	3216 x 2208
Frame Rate	1590 FPS	470 FPS	408 FPS	660 FPS	200 FPS
Sensor Format	**1/1.7" CMOS**	**1/1.7" CMOS**	**2/3" CMOS**	**1.1" CMOS**	**1.1" CMOS**
Pixel Size	9 µm	4.5 µm		9 µm	4.5 µm
Sensor: SONY High-Speed Image Sensor	IMX426	IMX422	IMX421	IMX425	IMX420
Interface	**10 Gigabit Ethernet SFP+ for fast data transmission**				
Programmable and Reconfigurable FPGA	Xilinx Zynq Ultrascale				

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	CAMERA FAMILY	SPINOSAURUS EVO				
IMAGING SENSOR	**Camera Model**	0.5	2.0	2.8	1.7	7.1
	Model (SONY)	IMX426	IMX422	IMX421	IMX425	IMX420
	Monochrome (M) Bayer Color (C)	M or C	M or C	M or C	M or C	M or C
	Diagonal mm	9.25 (1/1.7")	9.25 (1/1.7")	10.97 (2/3")	17.55 (1.1")	17.55 (1.1")
	Active Pixels H x V	**816 x 624**	**1632 x 1248**	**1944 x 1427**	**1608 x 1104**	**3216 x 2208**
	Frame Rate (Full Frame)	**1590 FPS**	**470 FPS**	**408 FPS**	**660 FPS**	**200 FPS**
	Pixel Size	9 µm	4.5 µm		9 µm	4.5 µm
	Dynamic Range	86 dB	80 dB		86 dB	80 dB
	ADC Resolution	**8/10/12 bit**				
	Analogue Gain	0-48dB at 0.1dB step				
	Region of Interest	YES, with 16 pixel increments				
	Shutter Type	Electronic global shutter				
	Shutter Time	5 us – 90 s				
	Pixel Clock Speed	1.9 Gpix/s (16 pixels @ 118.8 MHz)				
	Exposure	Linear, dual gain high dynamic range				
FEATURES	Pixel Correction	Dead pixel correction and programmable LUT				
	Trigger Modes	Free running, trigger, overlap and pulse width				
	Trigger Features	Delay 0 – 1000 ms, LP Filter 1.5Hz - 100 kHz				
	Shutter Resolution	1.56 us				
PROCESSING	FPGA	Xilinx Zynq Ultrascale+ ZU4CG				
	Free FPGA %	Up to 50%, most of 728 slices of DSP are free.				
	Volatile Memory	2 GB LPDDR4 with 9.6 GB/s bandwidth				
	Non-volatile Memory	64 MB QSPI flash, 8 GB eMMC				
MECHANICAL	Lens Mount	C-mount (1" 32G thread)				
	Temp Range	0 - 50°C				
	Mass	TBD				
	Protection	Up to IP67 with housing				
	Housing Material	CNC-machined aluminum, anodized				
	RoHS	RoHS compliant				
	Fixing Holes	4x M3 OEM / 5 x M6 on housing				
ELECTRICAL	Input Voltage	DC 9-36V or 5V (OEM)				
	Consumption	up to 30W				
	IO	20x 3.3V TTL ZIF				
	IO Isolation	3x IN / 3x OUT opto-isolated				
	Connectors	10G SFP+, 10 pin Hirose HR10A, ZIF or OEM				
FUNCTIONALITIES	On-board Image Processing	As an option (if an IP core is integrated)				
	Open Reference Design	**Yes**				
	Open Architecture	**Yes**				
	Software	Compatible with OptoMotive EVO software (full source included)				
	Operating System	Windows 7, Windows 10, 64bit or 32bit				
	Development Tools	Xilinx Vivado/SDK version 2018.2 or later. Microsoft Visual Studio 2017				